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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,421	02/02/2000	Ritsuko Iwasaki	24705/99	6172

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EXAMINER
LEE, EUGENE

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/496,421	IWASAKI, RITSUKO	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-9 and 11-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *3-9 and 11-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the element isolation region (claim 11) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. Figs. 6-8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "1" has been used to designate both "gate" and "source diffusion region". See page 7, line 1 and page 8, line 1.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 11, 12, 16 and 17 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not disclose dummy gate electrodes ***on*** element isolation regions.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12 recites the limitations "first transistor" and "second transistor" in line 1 of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 5, 14, 15, and 18 thru 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bush et al. '283. Bush discloses (see, for example, FIG. 5) a test structure comprising gate conductors (first and second gate) 20 and conductors (first and second dummy gate) 40. The first transistor (the second from the left in FIG. 5 of Bush) possesses a first gate 20, first source region 22 and first drain region 24 and is spaced from a first dummy gate (the third from the left) 40. The first dummy gate is laterally spaced from a second transistor (on the

far right) possessing a second gate 20, second source region 22 and second drain region 24. The second dummy gate 40 (on the far left) lies outside the first source regions and the first drain region. The first and second gates, and said first, second dummy gates are evenly spaced. Bush does not show a third dummy gate arranged adjacent to said second drain. However, it would have been obvious to one of ordinary skill in the art at the time of invention to include an additional dummy gate with more transistors in order to test more transistors within a single test structure.

10. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bush et al. '283 as applied to claims 3, 5, 14, 15 and 18 thru 25 above, and further in view of Ham '595. Bush does not disclose said first and second gates being respectively three forked. However, Ham shows (see, for example, FIG. 1) a NMOS transistor having a ladder structure where several gate branches G extend from a main line of a gate pattern 1. It was well known in the art at the time of invention to implement this ladder structure so that one could accommodate a greater number of transistors in a minimum amount of space. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a ladder structure of Ham for the reason cited above.

11. Claims 6 thru 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. '686 in view of Lin et al. '900. Mizuno discloses (see, for example, FIG. 21) a semiconductor device comprising multiple transistors wherein each transistor comprises a gate electrode, and source/drain regions coupled to overlying contact holes. The distances between the gate electrodes and the contact holes are substantially the same. Mizuno does not disclose said fourth electrode layer electrically coupled to aid second electrode layer. However, Lin discloses (see,

for example, FIG. 5B) a semiconductor device comprising transistors wherein the transistors' drain regions are connected together. It was well known in the art at the time of invention to connect drain regions of different transistors of the same device (i.e. CMOS) in order to share a signal between drain regions. See, for example, column 4, lines 52-65. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to connect the drain regions together in Mizuno's invention in order to share a common signal between different transistors.

12. Claims 9, 11, 12, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. '686 in view of Lin et al. '900 as applied to claims 6 thru 8 above, and further in view of Uehara et al. '563. Mizuno does not disclose dummy layers. Uehara, on the other hand, discloses (see, for example, Fig. 13e) dummy electrodes 50b surrounding the gate electrode 50a and the source/drain regions 21 of a transistor. The dummy electrodes reside above an isolation 17. Uehara teaches that including dummy layers will reduce variation in the length of the gate electrode and remove the need of extra margin for the displacement of masks. See, for example, column 19, lines 65-*. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the dummy layers of Uehara in Mizuno in view of Lin for the reasons cited above.

Response to Arguments

13. Applicant's arguments with respect to claims 3-9, and 11-25 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the Drawing Objection towards Figs. 6-8, the applicant's disclosure clearly states (see, for example, page 6, lines 9-14) these figures as conventional and prior art. Therefore, as stated above, Figs. 6-8 should be designated by a legend such as --Prior Art--.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
February 11, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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